UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,298	04/12/2004	Liping Ren	IR-2390 (2-3	4746

2352 7590 02/25/2008
OSTROLENK FABER GERB & SOFFEN
1180 AVENUE OF THE AMERICAS
NEW YORK, NY 100368403

EXAMINER	
PIZARRO CRESPO, MARCOS D	
ART UNIT	PAPER NUMBER
2814	
MAIL DATE	DELIVERY MODE
02/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,298	REN, LIPING	
	Examiner	Art Unit	
	Marcos D. Pizarro	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9,11,13 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,11,13 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Attorney's Docket Number: IR-2390 (2-3965)
Filing Date: 4/12/2004
Claimed Priority Date: 4/11/2003 (Provisional 60/462,562)
Applicant(s): Ren
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the request for reconsideration filed on 1/22/2008.

Acknowledgment

1. The request for reconsideration filed on 1/22/2008, responding to the Office action mailed on 10/15/2007, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1-7, 9, 11, 13, and 20-23.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9, 11, 13, and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujishima (US6740952) in view of Rumennik (US6639277), Van Zant, Ghandhi, Noda (US6617652), and Ranjan (US5801431).

4. Regarding claim 1, Fujishima shows (see, *e.g.*, figs. 15 and 19) most aspects of the instant invention including a semiconductor device comprising:

- ✓ A semiconductor substrate **1** of a first conductivity type
- ✓ A semiconductor layer of a second conductivity type formed over the substrate **1**
- ✓ A body region **2** of the first conductivity formed in the semiconductor layer
- ✓ An invertible channel in the body region **2**
- ✓ A source region **3** of the second conductivity type formed in the body region **2** and adjacent to the channel
- ✓ A gate structure formed over the channel region including:
  - a gate electrode **9**
  - a gate insulation layer **7** spacing the gate electrode **9** from the channel
- ✓ A drain region **6** formed in the semiconductor layer
- ✓ A drift region **5** in the semiconductor layer spacing the body region **2** from the drain region **6**
- ✓ A resurf region **20** of the first conductivity formed in the semiconductor layer of the second conductivity type, said resurf region **20** being formed over at least a portion of the drift region **5** between the body region and the drain region
- ✓ A field plate structure disposed over the drift region **5** including:
  - a first insulation layer **8** of a first thickness extending from the gate insulation layer
  - a second insulation layer **10** of a second thickness formed over the first insulation layer **8**

- a third insulation layer **25** of a third thickness
- a first plate **9** disposed over the first insulation layer **8**
- a second plate **FP1** disposed over the second insulation layer **8**
- a third plate **FP2/FP3** spaced from the second plate **FP1** by the third insulation layer **25**

Wherein:

- ✓ the first plate **9** includes a first portion extending from the gate electrode (see, *e.g.*, fig. 19)
- ✓ the second plate **FP1** includes (see, *e.g.*, fig. 19):
  - a first portion
  - a second portion
  - a second gap separating the portions
- ✓ the third plate **FP2** includes (see, *e.g.*, fig. 19):
  - a first portion
  - a second portion
  - a third gap **Wg** separating the portions
- ✓ the second gap is wider than the third gap **Wg** (see, *e.g.*, fig. 19)

3. Fujishima, however, fails to show the first plate including a second portion spaced from the first portion of the first plate by a first gap wider than the second gap. Rumennik (see, *e.g.*, figs. 1 and 2), on the other hand, shows a first plate similar to Fujishima including a first portion **12** spaced from a second portion **26** by a gap wider than the gap separating first and second portions **10,11** of a second plate above the first

plate. He further teaches that the second portion **26** would function to increase the breakdown voltage of Fujishima (see, *e.g.,* Rumennik/col.4/ll.42-45).

4. It would have been obvious at the time of the invention to one of ordinary skill in the art to include the second portion suggested by Rumennik in the first plate of Fujishima to reduce the field concentration at the boundary between the drain region and the drift region.

5. Fujishima also fails to show the semiconductor layer being epitaxially formed and extending below the body region. Rumennik, on the other hand, shows the semiconductor layer being epitaxially formed (see, *e.g.*, col.7/ll.21) and extending below the body region (see, *e.g.*, fig.5 and fig.6). Van Zant (see, *e.g.*, pp.382), on the other hand, teaches that epitaxially forming Fujishima's semiconductor layer would allow accurate control of the doping concentrations of the layer. Ghandhi (see, *e.g.*, pp.258) teaches that epitaxially forming Fujishima's semiconductor layer on the substrate would eliminate the problems of compatibility or mismatch between the layer and the substrate.

6. It would have been obvious at the time of the invention to one of ordinary skill in the art to epitaxially form Fujishima's semiconductor layer, as suggested by Van Zant and Ghandhi, to eliminate compatibility problems between the layer and the substrate and to accurately control the doping concentrations of the layer.

7. Fujishima fails to show the first and second portions of the second field plate, and the first and second portions of the third field plate being circular and disposed around the drain region. Noda, on the other hand, teaches (see, *e.g.*, fig. 1) that annular

circular plates formed concentrically around the drain diffusion region of Fujishima would improve the breakdown properties of the device (see, *e.g.*, Noda/col.14/ll.20-22 and col.9/ll.38). Ranjan elaborates by teaching that the series of plates in Noda reduce the tendency to concentrate high electric fields near the surface of the device thereby improving its breakdown voltage (see, *e.g.*, Ranjan/col.5/ll.52-56).

8. It would have been obvious at the time of the invention to one of ordinary skill in the art to form the first and second portions of the second and third plates of Fujishima/Rumennik as annular circular portions disposed around the drain region, as suggested by Noda and Ranjan, to further improve the breakdown voltage properties of the device.

9. Regarding claims 2, 4, and 6, Fujishima shows the first **8**, second **10** and third **25** insulation layers comprising an oxide (see, *e.g.*, fig. 19)

10. Regarding claim 3, Fujishima shows the first thickness is 0.6 microns (see, *e.g.*, col.36/ll.20) but fails to specify the claimed thickness of 0.4 microns. However, differences in thickness will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such thickness is critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

11. Fujishima also teaches that the first thickness, as well as the other thicknesses of the different insulation layers, affects the performance and the area of the device (see, *e.g.*, col.37/ll.15-29, col.8/ll.36-40, and col.39/ll.17-31). Therefore, it is necessary to

ensure that the insulation layers are of an appropriate thickness (see, e.g., Fujishima/col.35/ll.60-62). The specific claimed first thickness, *i.e.*, 0.4 microns, absent any criticality, is only considered to be the "optimum" thickness disclosed by Fujishima that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired device performance, manufacturing costs, etc. (see Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, *i.e.*, results which are different in kind and not in degree from the results of the prior art, will be obtained as long as the first thickness provides for a stable performance of the device, as already suggested by Fujishima.

12. Since the applicant has not established the criticality (see next paragraph) of the claimed thickness of 0.4 microns, it would have been obvious to one of ordinary skill in the art to use these values in the device of Fujishima.

CRITICALITY

13. The specification contains no disclosure of either the critical nature of the claimed thickness or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

14. Regarding claim 5, Fujishima shows the second thickness is 1.3 microns (see, *e.g.*, col.39/ll.5).

15. Regarding claim 7, Fujishima shows the third thickness is 2.5 microns (see, *e.g.*, col.39/ll.7) instead of the claimed thickness of 1.4 microns. See also the comments stated above in paragraphs 12-15 with respect to the differences between the claimed thickness and that of the prior art, which are considered repeated here.

16. Regarding claim 9, Fujishima shows the first field plate **9** comprising gate electrode material (see, *e.g.*, col.39/ll.9-10). Van Zant (see, *e.g.*, pp. 511), on the other hand, teaches that doped polysilicon is the standard gate electrode material for Fujishima's device.

17. Regarding claim 11, Fujishima shows that the gap between the portions of the second field plate **FP1** is 45 microns (see, *e.g.*, col.37/ll.29-34 and col.39/ll.13-16).

18. Regarding claim 13, Fujishima shows the third field plate **FP2** comprising a first portion and a second portion (see, *e.g.*, fig. 19), wherein a gap of 25 microns separates the portions (see, *e.g.*, col.37/ll.32).

19. Regarding claim 20, Fujishima shows the first portion of the first plate **9** terminating below the first portion of the second plate **FP1** (see, *e.g.*, fig. 19).

20. Regarding claim 21, Fujishima shows the second portion of the second field plate **FP1** is electrically connected to the drain region **6** and to the second portion of the third plate **FP2** (see, *e.g.*, fig. 19).

21. Regarding claim 22, Fujishima shows the first portion of the second plate **FP1** is electrically connected to the first plate **9** (see, *e.g.*, fig. 19).

22. Regarding claim 23, Fujishima shows the first portion of the third plate **FP2** is electrically connected to the source region **3** (see, *e.g.*, fig. 19).

Response to Arguments

23. The applicant argues:

24. In figure 15, Fujishima shows a p-type region **20** formed in the n-type drift region. However, Fujishima does not state that region **20** is a resurf region. Furthermore, the description of region **20** makes it unlikely that region **20** could serve as a resurf region. Therefore, region **20** would not function as a resurf region.

25. The examiner responds:

26. Applicant's arguments are mainly directed to functional aspects of the invention. The claims are, however, directed to a structure not to a function. The functional language is considered only in terms of a necessary resultant structure from the function. The function itself is not at issue. The device claims are not limited to the recited function. A limitation in a claim with respect to the manner in which a claimed device is intended to be used does not differentiate the claimed device from a prior-art device if the prior-art device shows all structural limitations of the claims. *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

27. In the instant case and as explained above in paragraphs 4-10, the cited prior art shows all structural aspects of the claimed semiconductor device. In fact, contrary to applicant's assertion, nothing in Fujishima's description would make region **20** unlikely to serve as a resurf region. See, *e.g.*, col.7/ll.57-61, where Fujishima teaches that as a result of forming the p-type region **20** in the n-type drift region **5**, the n-type region is provided with a high concentration, the high withstand-voltage is maintained, and the on-resistance is reduced. According to Kim (US6087232: see, *e.g.*, col.1/ll.56-65), Fujishima's p top layer helps the n drift region to be easily depleted even if the concentration of the concentration of the drift region is set high enough to reduce the on-resistance.

28. The applicant argues:

29. The recitation in claim 1 relates to the inherent structure and characteristics of a resurf region. Even if the limitation "resurf region" is considered functional, the structure implied by the "resurf region" limitation must be considered. Accordingly, reconsideration is required.

30. The examiner responds:

31. The examiner agrees with the applicant that the structure implied by the "resurf region" limitation should have been considered by the examiner even if the limitation is considered functional. The examiner did give full consideration to the "resurf region" limitation in the claim. See, *e.g.*, pp.4/ll.1-5 of the Office action mailed on 10/15/2007, where the examiner clearly makes reference to the p-top layer **20** of Fujishima as the resurf region. It is the understating of the examiner that the p-top layer of Fujishima is a resurf region and that is why throughout the Office action the examiner refers to said region as the resurf region.

32. In the response filed on 9/17/2007, the applicant stated that Fujishima did not refer to region **20** as a resurf region and that the description of region **20** makes it unlikely that region **20** could serve as a resurf region. The examiner disagreed and set forth his position regarding that argument. See, *e.g.*, paragraphs 29-31 of the Office action mailed on 10/15/2007.

33. Note that a limitation in a claim with respect to the manner in which a claimed device is intended to be used does not differentiate the claimed device from a prior-art device if the prior-art device teaches all structural limitations in the claims. *In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); *Ex parte Masham*, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See *Hewlett-Packard Co. v. Bausch & Lomb Inc.* and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a device claim, and not the patentability of its functions (909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990)). As stated in Best,

> Where the claimed and prior art products are identical or substantially identical in structure or composition, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA 1977).

34. **Note that the applicant has burden of proof** once the examiner establishes a basis for believing that the products of the applicant and the prior art are the same. See *In re Spada*, 911 F.2d 705, 709, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990).

35. Besides broadly stating that the claimed "resurf region" is structurally different from the prior art, the applicant has failed to set forth any structural differences between the claimed resurf region and the p-top layer **20** of Fujishima (see, *e.g.*, fig. 15). Accordingly, based on the prior art of record, one of ordinary skill in the art would have characterized Fujishima's p-top layer **20** as a resurf region.

36. The applicant argues:

37. It is not understood how Kim would make it likely for region **20** of Fujishima to be a resurf region.

38. The examiner responds:

39. Kim supports the examiner's characterization of region **20** of Fujishima as a resurf region. As set forth in Fujishima (see, *e.g.*, col.37/ll.57-61), the p-top layer allows providing the n-type drift region with a high concentration while maintaining the breakdown voltage and reducing the ON resistance of the transistor. Like Fujishima, Kim teaches increasing the concentration of the drift region to reduce the ON resistance of the transistor (see, *e.g.*, Kim: col.1/ll.57-65). But Kim teaches more. He teaches that even if the concentration of the drift region is set high enough to reduce the ON

resistance of the transistor, the p-top layer would help the n-type drift region to be easily depleted (see, *e.g.*, Kim: col.1/ll.57/65). One of ordinary skill in the art would have understood that this is precisely the function of a resurf region. This depletion occurs as a result of the interaction between the drift region and the p-top region (see, *e.g.*, Parthasarthy/col.1/ll.44-48).

40. Parthasarthy is still another teaching reference supporting the examiner's position that the p-top layer of Fujishima is a resurf region. As mentioned above, Fujishima clearly teaches that the p-top layer allows increasing the concentration of the drift region while maintaining the breakdown voltage and reducing the ON resistance of the transistor (see, *e.g.*, Fujishima: col.37/ll.57-61). According to Parthasarthy, Fujishima's transistor can maintain the breakdown voltage and reduce the ON resistance due to the depletion of the drift region caused by the resurf region (see, *e.g.*, Parthasarthy: col.1/ll.39-44). So, if anything, applicant's arguments on pp.7 of the response filed on 9/17/2007 saying that the p-top layer of Fujishima would cause the drift region to deplete actually supports the examiner's position as well as the teachings of the prior art that the p-top layer of Fujishima is a resurf region.

41. Parthasarthy and Kim are references teaching that the description of Fujishima does not make it unlikely for region **20** to be a resurf region, as argued by the applicant, but that on the contrary region **20** actually serves as a resurf region. Parthasarthy and Kim should not be construed as references changing the grounds of rejection of the present Office action.

Conclusion

42. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 10:00 AM to 8:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

44. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the

automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

45. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/335-343,409,487,488,491-493,659	2/15/2008
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	2/15/2008

/Marcos D. Pizarro/

Marcos D. Pizarro-Crespo
Primary Patent Examiner
Art Unit 2814
571-272-1716
marcos.pizarro@uspto.gov

MDP/mdp
February 27, 2008